The Chip-Scale Atomic Clock – Recent Developments

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***Abstract*—We report on recent advances in the core performance and capabilities of the Chip-Scale Atomic Clock.**

I. INTRODUCTION

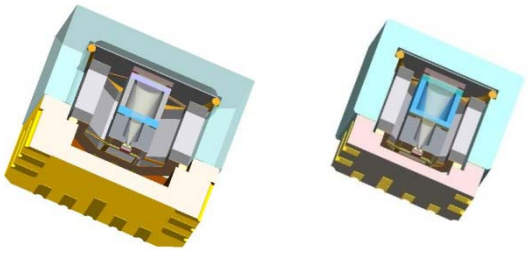
Atomic clocks play an essential role in the precise timing and synchronization of modern communications and navigation systems. Emerging Chip-Scale Atomic Clock (CSAC) technology will extend the network of atomic timing accuracy to portable, battery-powered applications.

Our research group at the Symmetricom Technology Realization Center, in collaboration with the Microelectromechanical Systems (MEMS) group at the Charles Stark Draper Laboratory and the optoelectronics group at Sandia National Laboratories[†], has been developing CSAC technology since 2002. At the 2005 IFCS, we presented our first demonstration of a fully integrated CSAC with power consumption < 200 mW and short-term stability $\sigma_y(\tau) < 1 \times 10^{-9}\tau^{-1/2}$[1]. At the 2007 EFTF/IFCS we reported on the performance consistency of 10 nearly-identical CSACs, with power consumption of ≈ 125 mW and short-term stability (STS) $\sigma_y(\tau) = 2 - 3 \times 10^{-10}\tau^{-1/2}$[2]. Since 2007, our engineering efforts have focused on updating the design for improved manufacturability, reliability, and consistency of build. This report describes iterative performance improvement and design features which have been implemented since our previous report.

II. CSAC OVERVIEW

A. Physics Package

The CSAC physics package architecture has been described in detail in previous publications [3,4] and is illustrated in **Figure 1**. Since 2007, the overall size of the physics package has been reduced from 1 cm^3 (**Figure 1 (a)**) to 0.35 cm^3 (**Figure 1 (b)**). Note that the geometry of the key performance-determining elements, the resonance cell, laser, and detector assembly has not been altered to preserve clock stability. Rather the volume of the empty vacuum space between the temperature-stabilized central assembly and the package has been reduced. The impact on power consumption is minimal as thermal conduction through the support assembly remains a small component of the overall power consumption, which is otherwise dominated by thermal radiation from the heated surfaces. The new smaller physics package operates at 90°C in 25°C ambient temperature with <10 mW of heater power.



(a) (b)

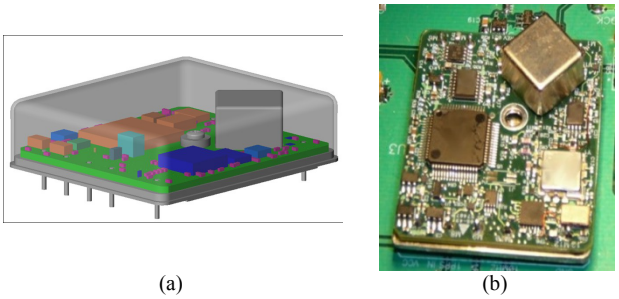
Figure 1: (a) 1 cm^3 and (b) 0.35 cm^3 CSAC Physics Packages

B. Electronics

The electronics architecture also remains largely unchanged from the prototype design. Iterative improvements include the implementation of a 1 pulse-per-second (PPS) system (see **Section IV**), migration to a higher-performing microprocessor, and other minor improvements to reduce power and improve performance. Significant effort has been spent refining the firmware to reduce power, improve performance, and ensure reliable operation over the expected range of environmental conditions.

C. Packaging

Minor improvements have also been made to the CSAC packaging. As shown in **Figure 2**, we have taken advantage of the smaller physics package to add a second layer of mu-metal shielding for reduced magnetic sensitivity, without increasing the overall CSAC dimensions.



(a) (b)

Figure 2: CSAC (a) solid model and (b) photograph

[†]Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.
This work is supported by the Defense Advanced Research Products Agency, Contract # W15P7T-08-C-P217.
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III. CSAC Performance

Significant performance improvements, since 2007, include a 25% reduction in the CSAC power consumption, 3X improvement in short-term stability, and remediation of the so-called "bimodal retrace problem."

A. Power Consumption

The overall power consumption of the CSAC has been reduced to less than 100 mW. Comparing **Table 1**, below, with **Table 1** of [2], the majority of the power savings have been realized through improvements in the efficiency of the microprocessor/firmware and the microwave synthesizer. Significant reduction in the required output power from the microwave VCO was accomplished by optimizing the coupling between the synthesizer and the physics package.

System	Component	Power
Signal Processing	MicroController	< 5 mW
	16-Bit DACs	12 mW
	Analog	8 mW
Physics	Heater Power	7 mW
	VCSEL Power	3 mW
	C-Field	0.5 mW
Microwave/RF	4.6 GHz VCO	25 mW
	PLL	18 mW
	10 MHz TCXO	7 mW
	Output Buffer	1 mW
1 PPS		< 0.5 mW
Power Regulation & Passive Losses		12 mW
Total		98 mW

Table 1: CSAC power consumption

B. Short-Term Stability

In 2007 we reported that the short-term stability (STS) of the 10 prototype CSACs was significantly degraded compared to the STS of the physics packages, when operated with optimal laboratory electronics. As shown in **Figure 11** of [5], the physics packages are capable of supporting STS of $\sigma_y(\tau) = 3 - 5 \times 10^{-11}\tau^{-1/2}$, while the complete CSACs only demonstrate $\sigma_y(\tau) = 2 - 3 \times 10^{-10}\tau^{-1/2}$, as shown in **Figure 8** of [2]. This 5-6X degradation was, at the time, attributed to additive electronic noise in the interrogation and/or signal recovery processes.

A focused effort has resulted in improvements in the signal recovery chain, the clock servo algorithms, and the microwave synthesizer. Individually these contributed only marginal improvement in the overall STS of the CSAC though, implemented together, they have resulted in 2-3X performance enhancement as illustrated in **Figure 3**.

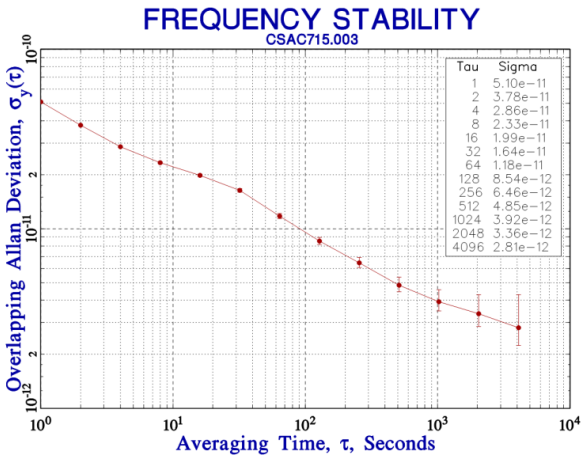


Figure 3: CSAC Short-term stability

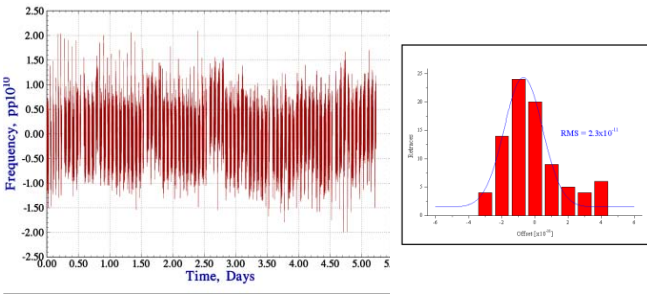
With improved electronics/firmware, typical CSAC STS is $\sigma_y(\tau) = 6 - 8 \times 10^{-11}\tau^{-1/2}$, a 2-3X improvement over previous results. Noting that this still does not realize the full potential of the physics package, we comment that further progress requires fundamental improvement in the noise properties of the microwave synthesizer.

C. Retrace

In **Figure 11** of [2] we presented disturbing results of the frequency "retrace" of the prototype CSACs, i.e. the frequency error measured when the CSAC was periodically powered on and off. The histogram of the retrace error showed a clear bimodal distribution. While each of the "modes" had a width of only $\Delta y=7\text{x}10^{-11}$, the spacing between the two modes was $y=2\text{-}3\text{x}10^{-10}$. The relative occurrence of the two modes seemed to be entirely random.

At the 2007 EFTF/IFCS, we postulated that the bimodal retrace was caused by the laser in the physics package acquiring initial lock on one of two polarization modes. Subsequent to that report, physics packages were built which incorporated a polarizer to ensure a single mode of operation. These devices displayed similar bimodal retrace.

Ultimately, the problem was traced to an uninitialized variable in the firmware and was resolved with the addition of a single line of source code.



(a) (b)

Figure 4: (a) Frequency measurement as CSAC was successively powered on for 2 hours and off for 1 hour. (b) histogram of measurements

Figure 4 shows the results of a recent retrace measurement. Over a period of 5 days, the CSAC was periodically cycled on for two hours and off for one hour. **Figure 4(b)** is a histogram of the frequency measurements over this period, indicating an overall retrace error of $\Delta y \approx 3 \times 10^{-11}$. Note that this data analysis necessarily includes errors due to long-term drift and temperature effects. Looking only at errors between adjacent cycles leads to a somewhat narrower distribution of $\Delta y = 1 \times 10^{-11}$.

D. Long-Term Drift

In 2007 we presented the long-term frequency behavior of one of the earliest CSAC engineering units, SN084, which, at that time, had been monitored for ≈200 days and exhibited drift of ≈ 3×10^{-11}/day. We continue to monitor the performance of SN084, which has now operated, nearly continuously, for nearly 1000 days.

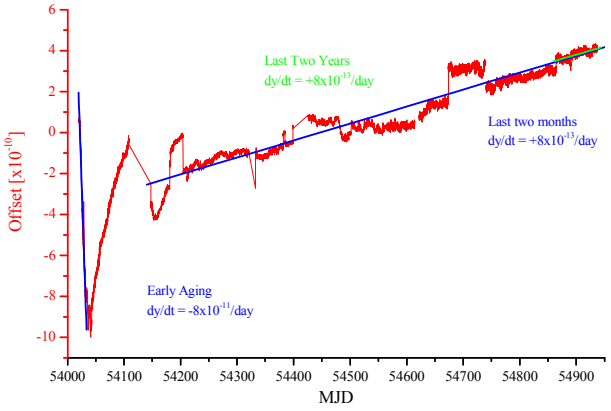


Figure 5: Long-term aging of SN084

Figure 5 shows the complete frequency data record of SN084. There are a number of "jumps" and outages due to power failures in our laboratory, equipment upgrades, etc. It is important to note, however, that the unit has never spontaneously lost lock. Over the past two years, the average frequency aging has been 8×10^{-13}/day (≈ 2.5×10^{-11}/month), which is consistent with the measurement over the most recent "continuous" interval, also 8×10^{-13}/day.

IV. 1 PULSE-PER-SECOND SYSTEM

In many potential applications the CSAC is employed as a long-term timing source, rather than as a frequency reference. Typically these applications require a precise 1 pulse-over-second (PPS) output from the CSAC and, ideally, a method for maintaining the time-of-day epoch (TOD). This permits the host system to remain powered down much of the time and only awaken when necessary for operations.

A. Synchronization and Timekeeping

The CSAC generates a 1 PPS output by digitally dividing the 10 MHz clock output by a factor of 10^7 and creating an output pulse every time the divider rolls over. A synchronous interrupt is generated to the microprocessor which increments the TOD variable. Upon request, the TOD value is reported via RS232, synchronous with the 1 PPS output, so that the host system can accurately associate the TOD with a particular epoch.

In order to synchronize the CSAC TOD with an external reference, such as output of a GPS receiver, a 1 PPS pulse is applied to the "1 PPS input" pin of the CSAC. The CSAC then resets the divide-by-10^7 counter so that the 1 PPS output is synchronous with the rising edge of the 10 MHz closest to the input 1 PPS. The accuracy of the synchronization is limited to +/- 50 ns by the (100 ns) period of the 10 MHz.

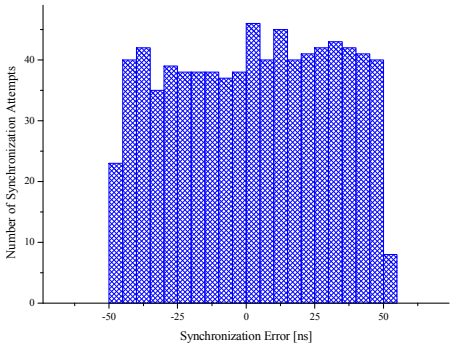


Figure 6: Histogram of synchronization accuracy to external 1 PPS input

Figure 6 shows the measured results of 800 attempts to synchronize to a pseudorandomly varying external 1 PPS pulse. As expected, the distribution is essentially flat-topped with error varying from -50 ns to +50 ns.

B. 1 PPS Time-Interval Measurement

We have implemented an analog phase interpolator for improved resolution of the time difference between the CSAC 1 PPS and the externally applied 1 PPS, beyond the 100 ns limit imposed by the 10 MHz counter. An analog voltage is generated by a simple integrate-and-dump circuit which is proportional to the time difference between the two 1 PPS pulses. The analog circuit provides a full-scale voltage equivalent to 2 µs, which is sampled by a 12-bit analog-to-digital converter (ADC), yielding an effective digitization resolution of $2\ \mu s/2^{12} \approx 500$ps. The addition of the phase interpolator adds 250 µW to the overall CSAC power budget.

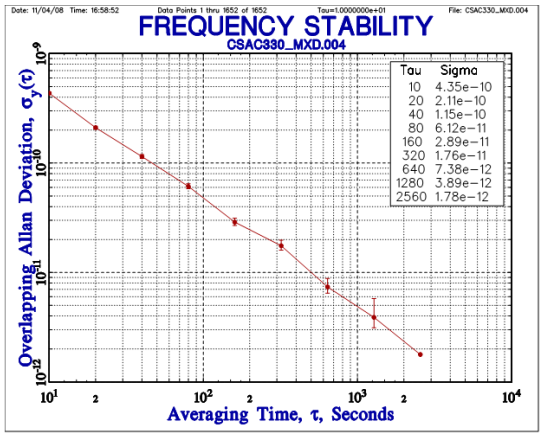


Figure 7: Phase interpolator self-test

Figure 7 shows the stability of a self-test of the phase interpolator, in which the output 1 PPS from the CSAC was connected to the 1 PPS input. The one-second intercept is $\sigma_y(\tau = 1) = 4 \times 10^{-10}$, indicating measurement resolution of ΔT=400 ps. With increasing averaging time, the stability improves $\sigma_y \propto \tau^{-1}$, i.e. as white phase noise, reflecting the digitization error of the ADC.

C. Calibration and Disciplining to 1 PPS

A proportional-integral (PI) loop filter, with an adjustable time constant, has been implemented in the CSAC firmware so that the CSAC can discipline itself, in both phase and frequency, to the external 1 PPS.

One application of the disciplining algorithm is to provide precise field calibration of the CSAC. If a 1 PPS reference source is available with superior stability to that of the CSAC, then the time for calibration is primarily limited by the stability of the CSAC, $\sigma_y(\tau) \approx 10^{-10}\tau^{-1/2}$.

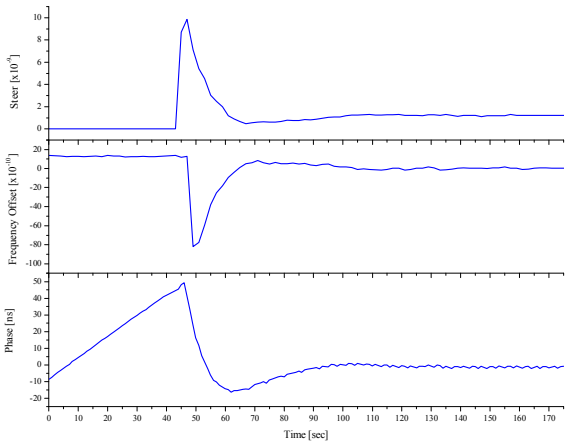


Figure 8: CSAC self-calibration to 1 PPS reference. Bottom: phase error. Middle: frequency error. Top: internal steering adjustment

Figure 8 shows an example of a CSAC calibrating itself to an externally-applied 1 PPS reference. In this case, the CSAC was deliberately mis-calibrated by $\Delta\bar{y} = 10^{-9}$ prior to the experiment. The 1 PPS reference was applied at T=40 seconds, after ≈ 50 ns of accumulated phase error. With the disciplining time constant set to τ = 5 s, the CSAC is calibrated to an accuracy of $\Delta\bar{y} < 10^{-11}$ and ΔΦ < 1 ns within 30 seconds.

Another useful application of the disciplining function is to enable the use of the CSAC as a GPS "holdover" or clean-up oscillator, in which the CSAC is served to the 1 PPS output of a GPS receiver in order to improve its short-term stability and provide continuity in the event of GPS failure.

In this case, the noise measured by the interpolator is dominated by the relatively poor stability of the GPS receiver, typically $\sigma_y(\tau) = 10^{-8}\tau^{-1}$. In order to avoid degrading the CSAC stability at short times, the disciplining time constant is set to $\tau \approx 5000$ sec, where the noise processes of GPS and CSAC intersect.

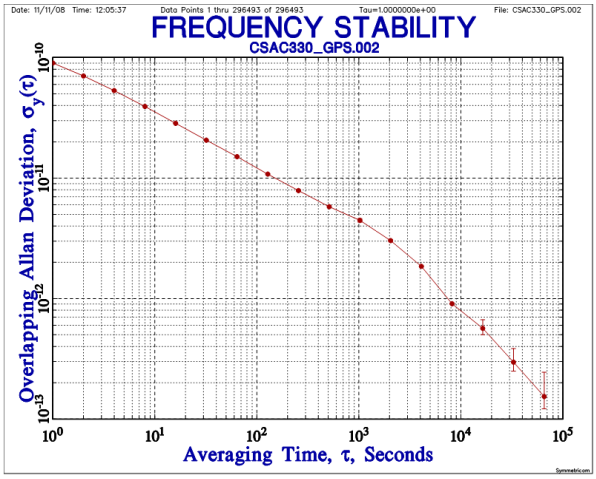


Figure 9: CSAC self-locked to GPS with 5000 second time constant

Figure 9 shows the stability of a CSAC locked to the 1 PPS output of a Novatel GPS receiver. For short averaging intervals, τ < 1000 seconds, the stability reflects the $\sigma_y(\tau) = 10^{-10}\tau^{-1/2}$ behavior of the CSAC. For longer averaging intervals, the stability reflects the $\sigma_y(\tau) = 10^{-8}\tau^{-1}$ behavior of the GPS receiver.

V. Ultra-Low Power Mode

The current CSAC implementation consumes less than 100 mW of power, enabling its use in a number of emerging applications requiring atomic timing in portable battery-powered applications. Nonetheless there are applications which require still lower power, particularly those requiring unattended sensing in remote locations. Typically, these applications exploit the long-term timing accuracy of the CSAC, rather than its short-term stability.

We have developed an ultra-low power (ULP) mode of operation for the CSAC. In ULP mode, the physics package controls and the microwave synthesizer are powered down for most of the time and the clock output is provided by the free-running TCXO. Periodically, the physics packaged is briefly powered up and the TCXO is recalibrated. In this fashion, the CSAC exhibits the short-term stability of a TCXO with the long-term drift characteristics of an atomic clock, with significantly reduced power consumption.

This approach to reducing power consumption was originally proposed in 1986 as the "RbXO" by W.J. Riley and J.R. Vaccarro [6] for conventional rubidium oscillators (RBO). The success of the RbXO was limited because stabilization of an RBO physics package takes a relatively long time (≈ 15 minutes) and high power (3X quiescent). This technique, however, is well-suited to the CSAC, which achieves lock in < 2 minutes and only requires ≈ 110 mW during initial acquisition.

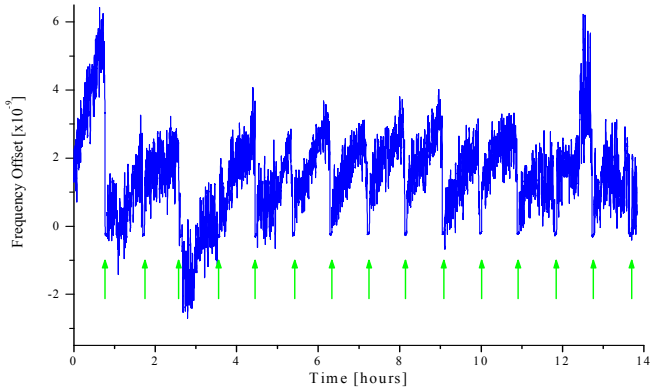


Figure 10: ULP CSAC. Green arrows indicate recalibration periods

Figure 10 is a frequency record of a CSAC operating in ULP mode. In this example, the physics and synthesizer are powered on for 4 minutes out of every hour. The green arrows in the figure indicate the ≈ 2-minute intervals during which the TCXO is locked to the physics. The time-averaged power of the CSAC operating in this mode is < 20 mW.

Figure 11 compares the accumulated timing error for a CSAC operating normally (green), operating in ULP mode (red), and operating with the TCXO open loop (blue). The data was taken with a single CSAC, only the operating mode was changed. For each measurement the clock was initially calibrated in both phase and frequency.

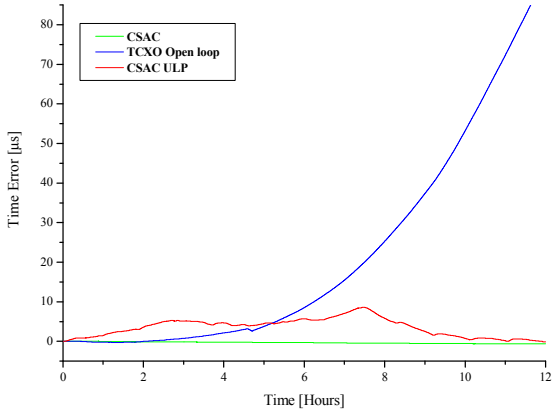


Figure 11: ULP CSAC accumulated timing error. Green: Normal CSAC operation. Red: ULP CSAC. Blue: TCXO open loop.

VI. Conclusion

Since our previous report at EFTF/IFCS 2007, we have continued to evolve the CSAC electronics and firmware. The overall power consumption of the CSAC has been reduced to < 100 mW. At the same time the short-term stability has been improved by 2-3X, the bimodal retrace problem has been eliminated, and we have added a 1 PPS input, output, and phase measurement system. We have demonstrated an ultralow-power mode of operation in which the CSAC displays the short-term stability of a free-running TCXO with the long-term stability of an atomic clock while consuming <20 mW of power.

Acknowledgments

The ongoing success of CSAC continues to benefit from its many outstanding contributors including, at least, S. Chang, D. Taylor, and T. Gebrewold of Symmetricom, M. Mescher, J. Leblanc, and G. Tepolt of the Charles Stark Draper Laboratory, and D.K. Serkland, K. Geib, and G.M. Peake of Sandia National Laboratories.

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